REMARKS

Claims 5-32 are pending in the present application. Claim 5 has been amended.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document in parent application Serial No. 09/574,109.

Claim Rejections-35 U.S.C. 102

Claims 5 and 28 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Suzuki reference (U.S. Patent No. 5,990,742). This rejection is respectfully traversed for the following reasons.

The differential input section of claim 5 includes in combination a differential circuit; a first current mirror circuit; a second current mirror circuit; and a circuit "that is connected to the first and second current mirror circuits and that is responsive to a voltage level of a signal output by the second current mirror circuit, so that a voltage level of a signal output by the first current mirror circuit becomes equal to the voltage level of the signal output by the second current mirror circuit". Applicant respectfully submits that the Suzuki reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that transistors Tr23-Tr28 in Fig. 6 of the Suzuki

reference can be interpreted as the circuit of claim 5. However, the circuit portion including transistors Tr23-Tr28 in Fig. 6 of the Suzuki reference is not responsive to a voltage level of a signal output by a second current mirror circuit, so that a voltage level of a signal output by a first current mirror circuit becomes equal to the voltage level of the signal output by the second current mirror circuit, as featured in claim 5.

Particularly, the Examiner has interpreted transistors Tr5 and Tr21 in Fig. 6 of the Suzuki reference as the first current mirror circuit of claim 5, wherein an output signal of this interpreted first current mirror circuit would presumably be provided at node N5. Moreover, the Examiner has interpreted transistor Tr6 and Tr22 of the Suzuki reference as the second current mirror circuit of claim 5, wherein an output signal of this interpreted second current mirror circuit would presumably be provided at node N6.

Applicant respectfully submits that the circuit portion in Fig. 6 of the Suzuki reference including transistors Tr23 – Tr28 is not disclosed as operable to make a voltage level at node N5 equal to a voltage level at node N6, responsive to the voltage level at node N6, as would be necessary to meet the features of claim 5. That is, the voltage levels at nodes N5 and N6 in Fig. 6 of the Suzuki reference would become equal responsive to equal potential at nodes N2 and N3 of the differential amplifier circuit, as described in column 8, lines 8-21, not responsive to a voltage level at node N6 (i.e., output signal of the interpreted second current mirror circuit). Accordingly, Applicant respectfully submits that the differential input section of claim 5 distinguishes over the Suzuki reference as relied upon by the Examiner, and that this rejection,

insofar as it may pertain to claim 5, is improper for at least these reasons.

The differential input section of claim 28 includes in combination a differential circuit; a first current mirror circuit; a second current mirror circuit; and a feedback circuit "connected to the output nodes of the first and second current mirror circuits, wherein a voltage of the output node of the second current mirror circuit is supplied to the output node of the first current mirror circuit". Applicant respectfully submits that the Suzuki reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted the circuit portion including transistors Tr23 – Tr28 in Fig. 6 of the Suzuki reference as the feedback circuit of claim 28. However, the circuit portion including transistors Tr23 – Tr28 in Fig. 6 of the Suzuki reference is not disclosed as supplying a voltage at output node N6 of the interpreted second current mirror circuit to output node N5 of the interpreted first current mirror circuit, as would be necessary to meet the features of claim 28. In contrast, as described in column 6, lines 47-49 of the Suzuki reference, an output signal Vout delivered from the output terminal To is fed back to the gate of transistor Tr4 of the differential amplifier circuit, as input signal Vin2. Accordingly, Applicant respectfully submits that the differential input section of claim 28 distinguishes over the Suzuki reference as relied upon by the Examiner, and that this rejection is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 30-32

are allowed.

Applicant also respectfully notes the Examiner's acknowledgment that claims 6-27 and 29 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form. Applicant however respectfully submits that these above noted claims distinguish over the relied upon prior art at least by virtue of dependency upon claims 5 and 28 respectively, and that amendment of these claims to be in independent form is therefore unnecessary.

Conclusion

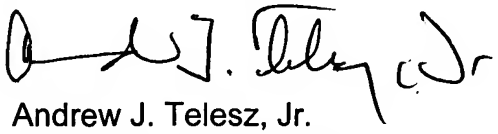
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass all the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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